



9.2.2.9 Definition of memory retention areas for bit memory. ... WinCC (TIA Portal) is an engineering software for configuring SIMATIC panels, SIMATIC. Read more9.2.2 Definition of retention memory areas for bit memory. 9.2.2.3 Definition of memory retention areas for RAM. 9.2.2.4 Defining retention areas for permanent memory. 9.2.2.5 Definition of retention areas for data memory. 9.2.2.6 Definition of retention areas for data memory with intermediate storage. ... WinCC (TIA Portal) is an engineering software for configuring SIMATIC panels, SIMATIC. Read more9.2.2.6 Definition of retention memory areas for data memory with intermediate storage. A retention area is an area of memory used to store data and commands. The size of the retention depends on the type and size of the data. Different memory areas with different names are used for storing data and commands: data memory (STORAGE), operating memory (MEMORY), memory cache (CASH), data memory with intermediate storage (RECOMMENDED SECURE). RECOMMENDED SECURE memory. Cache memory is an example of a memory with intermediate storage. All data written to a cache memory will be automatically copied to the RAM. When reading or writing from such memory the data will be immediately copied to the OP. Memory with intermediate storage can increase system performance and improve data security. The following types of cache memory are commonly used in the design of computing systems: - Direct-mapped (direct-mapped) data memory. This is a memory with which the processor directly exchanges data. The communication is in the form of sequential data reads and writes. The processor can read and write multiple bytes and therefore multiple words at a time. Each data byte has its own unique address in the data memory. The exchange is done with special readers, the latch register and the bay register. The address of the cache line stored in the latch register coincides with the address in the bay registers. Reading a write from the latch registers and reading a write from the bay registers is done in reverse. Since lines in the cache are nested, when the order of lines in the cache is changed, the addresses of the lines that were in the latch registers (and vice versa) will be preserved in the latch registers. Consequently, when accessing a specific line in the cache in the direct memory access mode, its address in the latches will coincide with the address of that line in the register slots. And vice versa, when accessing a line in the register-bay, its address in the cache-memory will coincide with the address of this line in the latch registers. This provides the simplest implementation of the direct memory access mode. The scheme of direct memory access with the use of cache memory is shown in Fig. D'3. Two methods can be used to access the cache memory in the direct memory access mode. In the first method (Fig. B4,a), each line in the cache is placed in one of the two registers-bays.

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